

WHAT IS CLAIMED IS:

1 1. An image sensor, comprising:
2 multiple pixels each including a respective photodiode region;
3 pixel circuits each operable to control integration and readout steps for a
4 respective pixel; and
5 a bias circuit operable to apply voltages across the pixels to induce carrier
6 injection into the photodiode regions to reduce image lag.

1 2. The image sensor of claim 1, wherein the bias circuit is operable to
2 induce forward bias flow of injected carriers through the pixel photodiode
3 regions.

1 3. The image sensor of claim 2, wherein the bias circuit is operable to
2 periodically induce forward bias flow of injected carriers through photodiode
3 regions.

1 4. The image sensor of claim 3, wherein the pixel circuits and the bias
2 circuit are cooperatively configured so that forward bias flow of injected carriers
3 occurs during a reset step for each pixel.

1 5. The image sensor of claim 2, wherein pixels are arranged in an
2 array of multiple rows and the bias circuit is operable to simultaneously induce
3 forward bias flow of injected carriers through the photodiode regions of all pixels
4 in a given row of the array.

1 6. The image sensor of claim 5, wherein the bias circuit is operable to
2 simultaneously induce forward bias flow of injected carriers through the
3 photodiode regions one row at a time.

1 7. The image sensor of claim 6, wherein the bias circuit is operable to
2 simultaneously induce forward bias flow of injected carriers through photodiode
3 regions of a given row before the pixel circuits in the given row initiate an
4 integration step for the given row.

1 8. The image sensor of claim 5, wherein the bias circuit is operable to
2 simultaneously induce forward bias flow of injected carriers through photodiode
3 regions of all rows in the array.

1 9. The image sensor of claim 1, wherein the bias circuit is operable to
2 induce carrier injection between photodiode regions of pixels.

1 10. The image sensor of claim 10, wherein the bias circuit is operable to
2 induce carrier injection between photodiode regions of adjacent pixels.

1 11. The image sensor of claim 10, wherein the bias circuit is operable to
2 apply different voltages levels to nodes of adjacent pixels.

1 12. The image sensor of claim 11, wherein the bias circuit is operable to
2 apply different high-to-low voltage ranges across adjacent pixels.

1 13. The image of sensor of claim 11, wherein pixels are arranged in an
2 array of multiple rows and the bias circuit is operable to apply different voltage
3 levels to nodes of adjacent pixels in adjacent rows.

1 14. The image sensor of claim 11, wherein pixels are arranged in an
2 array of rows and columns and the bias circuit is operable to apply different
3 voltage levels to nodes adjacent pixels in adjacent rows and to apply different
4 voltage levels to nodes of adjacent pixels in adjacent columns.

1 15. The image sensor of claim 10, wherein the different voltage levels
2 applied to nodes of adjacent pixels are switched periodically.

1 16. The image sensor of claim 10, wherein the bias circuit includes two
2 bias lines for applying different respective voltage levels to the pixels.

1 17. The image sensor of claim 10, wherein the bias circuit includes a
2 bias line and a set of resistive elements respectively coupled in parallel between
3 the bias line and alternate pixels.

1 18. A method of operating an image sensor comprising multiple pixels
2 each including a respective photodiode region, the method comprising:

3 resetting photodiode regions;
4 integrating charge in photodiode regions;
5 sampling pixel nodes; and
6 inducing carrier injection into photodiode regions to reduce image lag.

1 19. The method of claim 18, wherein inducing carrier injection
2 comprises inducing forward bias flow of carriers through the pixel photodiode
3 regions.

1 20. The method of claim 18, wherein inducing carrier injection
2 comprises inducing carrier injection between photodiode regions of adjacent
3 pixels.